



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,894	10/26/2001	John Erik Lindholm	NVIDP011A/P000094	7963
23419	7590	01/16/2004		
COOLEY GODWARD, LLP 3000 EL CAMINO REAL 5 PALO ALTO SQUARE PALO ALTO, CA 94306			EXAMINER HAVAN, THU THAO	
			ART UNIT	PAPER NUMBER
			2672	
			DATE MAILED: 01/16/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/032,894

Applicant(s)

LINDHOLM ET AL.

Examiner

Thu-Thao Havan

Art Unit

2672

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 24-35,40 and 41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 24-35,40 and 41 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 24-35 and 40-41 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims **24-35 and 40-41** are rejected under 35 U.S.C. 102(e) as being unpatentable by Krech, Jr (US patent no. 6,184,902).

Re claim **24**, Krech discloses a lighting system for graphics processing (col. 1, lines 48-67), comprising at least one input buffer adapted for being coupled to a transform system for receiving vertex data therefrom (fig. 5), a multiplication logic unit coupled to the at least one input buffer (fig. 3—element 55), an arithmetic logic unit coupled to the at least one input buffer and the multiplication logic unit (col. 3, lines 22-34), a register unit coupled to the arithmetic logic unit (col. 14, lines 28-55), and a lighting logic unit coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit (col. 3, lines 22-34; figs. 3-5). In other words, Krech teaches architecturally, the geometry accelerator includes a plurality of processing elements

(e.g., an arithmetic logic unit, a multiplier, a divider, a compare mechanism, a clamp mechanism, etc.) and a plurality of control units (e.g., a transform mechanism, a decomposition mechanism, a clip mechanism, a bow-tie mechanism, a light mechanism, a classify mechanism, a plane equation mechanism, a fog mechanism, etc.) that utilize the processing elements for performing data manipulations upon image data. In that each of the individual control unit logic elements situated within the control unit logic assists a corresponding control unit in accomplishing branching and indirect addressing. Each of the individual control unit logic elements is configured to make logical decisions for its respective control unit based upon and as a function of state data, including in the preferred embodiment, two least significant bits (LSBs) of the next address from the current instruction of the ROM, the branch field from the current instruction of the ROM, a condition code from the current instruction of the ROM, last vertex and light signals from a vertex/light counter indicative of whether or not the current instruction involves the last vertex and last light to be processed in a grouping of vertices/lights associated with a code subroutine, and the flags from the stack.

Re claim **25**, Krech discloses multiplication logic unit has a feedback loop coupled to an input thereof (col. 11, line 45 to col. 13, line 15; fig. 7). In other words, Krech teaches a vertex looping routine is commenced, which processes data associated with a vertex of the primitive during each loop operation. The appropriate control unit logic element determines via the last vertex bit whether the vertex that was recently operated on in the past by the stack is the last vertex of the primitive that is currently at issue.

Re claim **26**, Krech discloses lighting logic unit is coupled to the multiplication logic unit via a conversion module adapted for converting scalar vertex data to vector vertex data (fig. 5).

Re claim **27**, Krech discloses arithmetic logic unit and the multiplication logic unit include multiplexers (col. 3, line 15 to col. 4, line 41). Krech teaches in architecture, the geometry accelerator includes a plurality of processing elements (e.g., an arithmetic logic unit, a multiplier, a divider, a compare mechanism, a clamp mechanism, etc.) and a plurality of control units (e.g., a transform mechanism, a decomposition mechanism, a clip mechanism, a bow-tie mechanism, a light mechanism, a classify mechanism, a plane equation mechanism, a fog mechanism, etc.) that utilize the processing elements for performing data manipulations upon image data. In accordance with the invention, the control units are implemented in a read-only memory (ROM) via microcode instructions.

Re claims **28-29**, Krech discloses multiplication logic unit includes three multipliers coupled in parallel and arithmetic logic includes three adders coupled in series and parallel (col. 5, lines 14-45; col. 14, lines 13-48; figs. 4-5). In figure 4, Krech discloses the implementation enables multiway logic branching, which further enhances performance. In other words, multiple decisions can be made at the same time and in parallel. Moreover, the data path control field, which is passed to the stack from the ROM on connection, causes the ALU 54 (figure 5) to execute by adding operands A and B. Operands A and B are retrieved from the registers and/or RAM, the location of which is defined in the data path control of the instruction.

Re claims **30 and 34**, the limitations of claims 30 and 34 are identical to claim 24 above except for a memory. Therefore, claims 30 and 34 are treated the same as discussed with respect to claim 24 above. Krech's teaching is a computer graphics systems implemented in a read-only memory. It is apparent that a read-only memory is a memory.

Re claim **31**, Krech discloses memory includes a plurality of constants for processing the vertex data (col. 14, line 39 to col. 15, line 4).

Re claims **32-33**, Krech discloses memory has a read terminal coupled to the multiplication logic unit (fig. 4). Krech teaches Read-only memory. In that he discloses Figure 4 is an electronic block diagram showing a geometry accelerator of the invention having control units implemented in a read-only memory (ROM) and branch logic configured to assist instruction branching within the ROM.

Re claims **35 and 40-41**, the limitations of claims 35 and 40-41 are identical to claim 24 above except for a flag. Therefore, claims 35 and 40-41 are treated the same as discussed with respect to claim 24 above. Krech's teaches the processing elements are configured to provide flags (10 bits) to the branch logic (col. 6, line 53 to col. 7, line 9; fig. 6). Each microcode instruction residing in the ROM has at least the fields set forth in figure 6. Referring to figure 6, each instruction includes a branch field, a next address field, a next vertex field, a next light field, an init flag field, a data path control (instruction) field, a condition code field, and an operational control unit identification (ID) field.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Krech, Jr et al., US patent no. 5,930,519

Takeda et al., US patent no. 5,748,198

Rossin et al., US Patent No. 5,886,711

Gonzalex-Lopez et al., US Patent No. 4,866,637

Harris et al., US Patent No. 6,097,395

Inquiries

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thu-Thao Havan whose telephone number is (703) 308-7062. The examiner can normally be reached on Monday to Thursday from 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on (703) 305-4713.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Art Unit: 2672

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Thu-Thao Havan
Art Unit: 2672
December 29, 2003

A handwritten signature in black ink, appearing to read 'MRZ', with a long horizontal line extending to the right.

MICHAEL RAZAVI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600